Amendments to the Drawings:

The attached sheet of drawings includes changes to Figure 1. This sheet, which includes Figure 1, replaces the original sheet including Figure 1.

REMARKS

Claims 1-31 are presented for further examination. Claims 1 and 10 have been amended. Claims 16-31 are new.

In the first Office Action mailed January 11, 2005, the Examiner objected to Figure 1 because it should be designated by a legend such as "Prior Art." Applicants are submitting herewith a substitute formal Figure 1 with the legend "Prior Art" inserted thereon. Approval and entry of this substitute formal figure is respectfully requested.

Turning to the merits, claims 1, 9, 11, and 13 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,486,820 ("Allworth et al."). Claim 10 was allowed, and claims 2-8 and 14-15 were found to be allowable if rewritten into independent form to include the limitations of the base claim and any intervening claims.

Applicants respectfully disagree with the basis for the rejection and request reconsideration and further examination of the claims.

Turning first to the reference cited by the Examiner, Allworth et al., U.S. Patent No. 6,486,820, describe a pipeline analog-to-digital converter with a common mode following reference generator. As described by Allworth et al. at column 2, lines 49-66, a low-power operational amplifier has a limited dynamic range, and the common mode voltage of the amplifier may vary by a substantial fraction of the supply voltage. Allworth et al. propose to control one or more reference voltages for the stages of a pipeline ADC by including a reference generator to generate one or more reference voltages for the stages.

More particularly, the Allworth et al. reference generator (417) has a circuit to track the inherent common mode voltage of differential amplifiers such that a generated reference voltage (413) is relative to the inherent common mode voltages of the differential amplifiers in each of the stages. Figures 8A and 8B of Allworth et al., as described at column 11, line 38 through column 12, line 55, show generation of a common mode voltage for controlling various reference voltages and a current generated by a reference current generator (819) that passes through a current digital-to-analog converter (817). The reference generator is configured to track the inherent common mode voltage of the differential amplifiers in each of

the stages. Nowhere do Allworth et al. teach or suggest weighting each of the output signals from each of the stages according to a digital weight that depends on a corresponding inter-stage gain as does the present invention. Moreover, there is no teaching or suggestion in Allworth et al. of dynamically estimating a digital correction signal indicative of an analog error of a corresponding inter-stage gain and controlling the digital weight according to the digital correction signal.

Turning to the claims, claim 1 is directed to an analog-to-digital converter with a pipeline architecture for converting an analog input signal into a digital output signal. Claim 1 recites, inter alia, means for combining digital local signals of all the stages into the digital output signal, weighting each digital local signal according to a digital weight depending on the corresponding inter-stage gain. Claim 1 further recites means for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain and means for controlling the digital weight according to the digital correction signal.

As discussed above, nowhere do Allworth et al. teach or suggest such a means for combining digital local signals of the stages. First, in the present invention, the problem of reducing the distortion in the digital signal generated by the converter stages caused by the analog error in the inter-stage gain (see page 1, line 20 through page 2, line 8 of the present specification). In order to solve this problem, claim 1 proposes the idea of dynamically estimating a digital correction signal corresponding to the analog error of one or more inter-stage gains; the digital weights associated with these analog inter-stage gains are then updated according to the corresponding digital correction signals.

In contrast, Allworth et al. relate to a completely different problem as discussed above, *i.e.*, controlling the reference voltages of the stages relative to the inherent common mode voltages of the operational amplifiers in the stages (see Allworth et al. at column 3, lines 28-31). Thus, Allworth et al. describes the use of a dedicated reference generator (417) that includes a common mode generator (803) mimicking the common mode generation of all the differential amplifiers in the operational amplifiers (as described at column 11, lines 38-56). More particularly, the common mode generator (803) is formed by an instance of one-half of the differential amplifier (see Allworth et al. at column 11, lines 57-65).

In sharp distinction, the combination of claim 1 dynamically determines a digital correction signal corresponding to an analog error, and this requires a real-time measurement (for example, by means of the digital test signal t) for estimating the actual analog error that is introduced by the inter-stage gain. Nowhere do Allworth et al. teach or suggest such a solution as recited in claim 1. Applicants respectfully submit that claim 1 is clearly allowable over Allworth et al.

Claim 11 is directed to an analog-to-digital converter that recites, inter alia, a combining circuit for combining digital local output signals of all the stages into a digital output signal, weighting each local digital output signal according to a digital weight depending on the corresponding inter-stage gain, and for at least one of the stages a circuit for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain and a circuit for controlling the digital weight according to the digital correction signal. The combining circuit recited in claim 11 includes the features discussed above with respect to the means for combining the digital local signals of claim 1. Claim 13, which is also directed to an analog-to-digital converter, also recites a combining circuit that has features corresponding to those recited in claims 1 and 11. Applicants respectfully submit that claims 11 and 13, as well as all claims depending therefrom, are clearly allowable for the reasons why claim 1 is allowable.

New claims 16-23 are in essence allowable dependent claims 2-9, with claim 16 consisting of allowable dependent claim 2 in combination with claim 1. New claim 24 is allowable claim 14 rewritten into independent form to include the limitations of independent claim 13. Applicants respectfully submit that independent claims 16 and 24, as well as dependent claims 17-23 and 25 are allowable.

New claim 26 is directed to a circuit that recites features found in allowable claim 14, *i.e.*, a digital test signal generator for inserting a test signal into at least a first stage, an amplifier having an input coupled to an output of the first stage and an output coupled to an adder, a second amplifier having an input coupled to the first stage and having an output coupled to a circuit for controlling the digital weight and having an output coupled to the adder, the adder having an input coupled to an output of the combining circuit and an output coupled to an output

of the converter and to an input of a circuit for correlating the digital test signal with local digital signals of the stages that have an output coupled to the circuit for controlling the digital weight. Applicants respectfully submit that claim 26 and dependent claims 27-28 are allowable for the reasons why claim 14 was found to be allowable.

New claims 29-31 are directed to a method for converting an analog input signal into a digital output signal that includes the steps of combining the local digital output signals of all the stages into the digital output signal, weighting each digital local signal according to a digital weight depending on the corresponding inter-stage gain, and, for at least one of the stages, dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain, and controlling the digital weight according to the digital correction signal. Claim 29 includes the steps found in allowable claim 10 for combining digital local signals of all the stages, and weighting each digital local signal according to a digital weight, dynamically estimating a digital correction signal, and controlling the digital weight according to the digital correction signal. Applicants respectfully submit that claim 29, as well as dependent claims 30-31, are allowable for the reasons why claim 10 is allowable.

In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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ERT:jl

Enclosure:
Postcard
1 Sheet of Drawings (Figure 1)

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